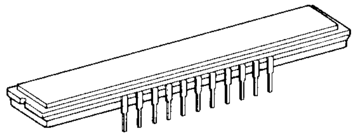
Preliminary

TOSHIBA CCD Linear Image Sensor
CCD (charge coupled device)

TCD2704D

The TCD2704D is a high sensitive and low dark current 7500 elements × 4 line CCD color image sensor which includes CCD drive circuit, clamp circuit.

The sensor is designed for scanner. The device contains a row of 7500 elements × 4 line photodiodes which provide a 24 lines/mm across a A3 size paper. The device is operated by 5 V pulse and 12 V power supply.



WDIP22-G-400-2.54D (H)

Weight: 5.2 g (typ.)

Features

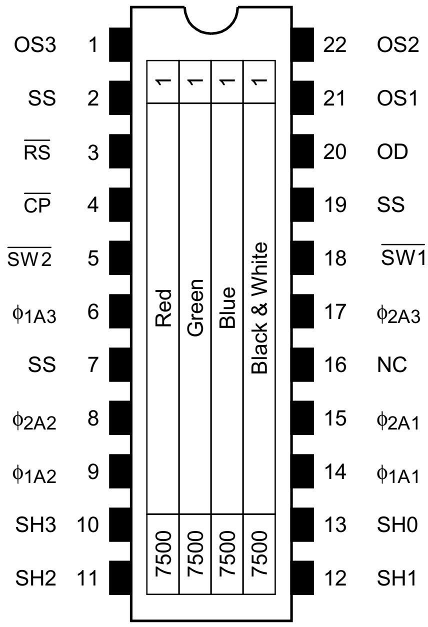
- Number of image sensing elements: 7500 elements × 4 line
- Image sensing element size: 5 μm × 5 μm on 5 μm centers
- Photo sensing region: High sensitive PN photodiode
- Distanced between photodiode array: Color (40 μm, 8 lines), B/W-color (60 μm, 12 lines)
- Clock: 2 phase (5 V)
- Power supply: 12 V power supply voltage
- Internal circuit: Clamp circuit
- Package: 22 pin CERDIP package
- Color filter: Red, green, blue

Maximum Ratings (Note 1)

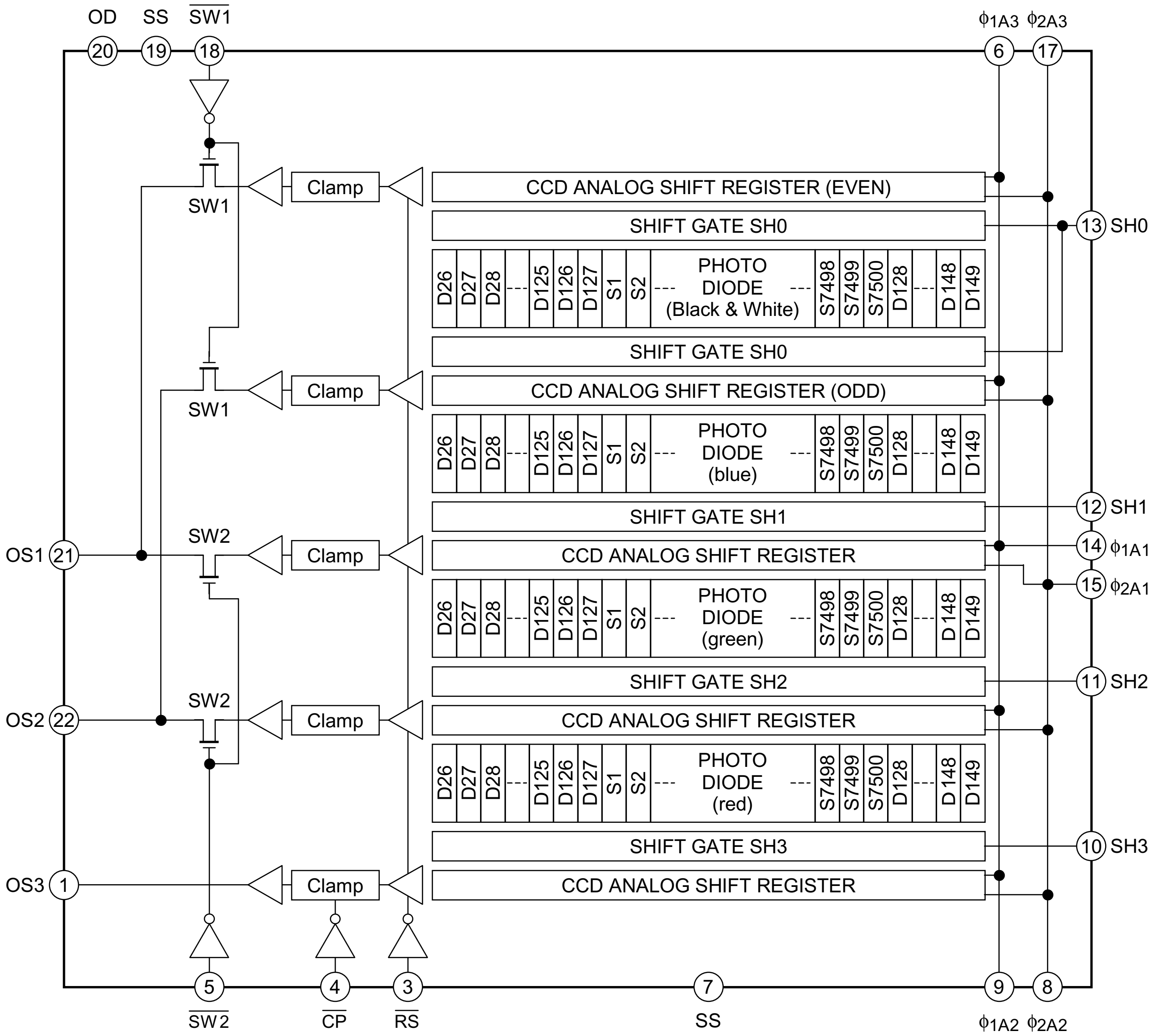
Characteristic	Symbol	Rating	Unit
Clock pulse voltage	V_{ϕ}	–0.3~8.0	V
Shift pulse voltage	V_{SH}		V
Reset pulse voltage	$V_{\overline{RS}}$		V
Clamp pulse voltage	$V_{\overline{CP}}$		V
Changeover switch voltage	$V_{\overline{SW}}$		V
Power supply voltage	V_{OD}	–0.3~15	V
Operating temperature	T_{opr}	0~60	°C
Storage temperature	T_{stg}	–25~85	°C

Note 1: All voltage are with respect to SS terminals (ground).

Pin Connections (top view)



Circuit Diagram



Pin Names

OS3	Signal Output 3 (red)	OS2	Signal Output 2 (green)
SS	Ground	OS1	Signal Output 1 (blue)
$\overline{RS}$	Reset Gate	OD	Power
$\overline{CP}$	Clamp Gate	SS	Ground
$\overline{SW2}$	Changeover Switch 2 (color and B/W)	$\overline{SW1}$	Changeover Switch 1 (color and B/W)
ϕ_{1A3}	Clock 3 (phase 1)	ϕ_{2A3}	Clock 3 (phase 2)
SS	Ground	NC	Non Connection
ϕ_{2A2}	Clock 2 (phase 2)	ϕ_{2A1}	Clock 1 (phase 2)
ϕ_{1A2}	Clock 2 (phase 1)	ϕ_{1A1}	Clock 1 (phase 1)
SH3	Shift Gate 3	SH0	Shift Gate 0
SH2	Shift Gate 2	SH1	Shift Gate 1

Optical/Electrical Characteristics

(Ta = 25°C, V_{OD} = 12 V, V_{ϕ} = V_{RS} = V_{SH} = V_{CP} = 5 V (pulse), f_{ϕ} = 1.0 MHz, f_{RS} = 1.0 MHz, LOAD RESISTANCE = 100 kΩ, t_{INT} (INTEGRATION TIME) = 10 ms, LIGHT SOURCE = A LIGHT SOURCE + CM500S FILTER (t = 1.0 mm))

Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Sensitivity	$R_{B/W}$	8.6	10.8	13.0	V/(lx･s)	(Note 2)
	R_R	3.2	4.6	6.0		
	R_G	3.7	5.4	7.1		
	R_B	1.9	2.8	3.7		
Photo response non uniformity	PRNU (1)	—	10	20	%	(Note 3)
	PRNU (3)	—	3	12	mV	(Note 4)
Image lag	IL	—	1	—	%	(Note 5)
Saturation output voltage (B/W)	$V_{SAT\ (B/W)}$	1.5	2.0	—	V	(Note 6)
Saturation output voltage (color)	$V_{SAT\ (color)}$	2.0	2.5	—	V	(Note 6)
Saturation exposure	SE	—	0.19	—	lx･s	(Note 7)
Dark signal voltage	V_{DRK}	—	0.4	2.0	mV	(Note 8)
Dark signal non uniformity	DSNU	—	7	12	mV	(Note 8)
DC power dissipation	P_D	—	525	650	mW	—
Total transfer efficiency	TTE	92	—	—	%	—
Output impedance	Z_O	—	0.3	1.0	kΩ	—
DC signal output voltage	V_{OS}	5.0	6.0	7.0	V	(Note 9)
Random noise	$N_{D\sigma}$	—	1.0	—	mV	(Note 10)
Reset noise	V_{RSN}	—	0.5	1.0	V	(Note 9)

Note 2: Sensitivity is defined for each color of signal outputs average when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

Note 3: PRNU (1) is defined for each color on a single chip by the expressions below when the photosensitive surface is applied with the light of uniform illumination and uniform color temperature.

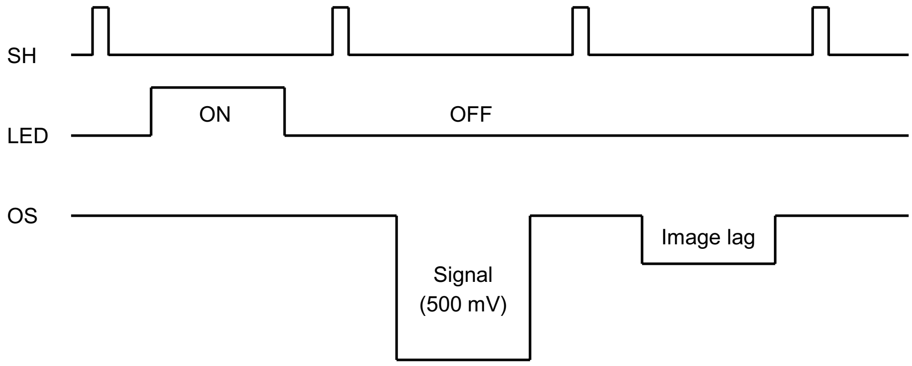
$$\text{PRNU (1)} = \frac{\Delta X}{\overline{X}} \times 100\ (\%)$$

When $\overline{X}$ is average of total signal output and ΔX is the maximum deviation from $\overline{X}$. The amount of incident light is shown below.

$$\text{Ped} = \frac{1}{2}\ \text{SE, Green} = \frac{1}{2}\ \text{SE, Blue} = \frac{1}{4}\ \text{SE}$$

Note 4: PRNU (3) is defined as maximum voltage with next pixel, where measured 5% of SE (typ.)

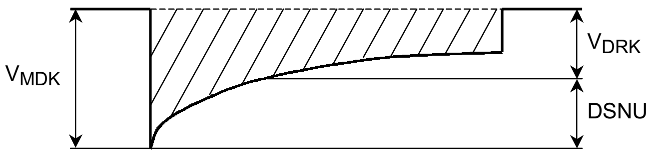
Note 5: Image lag is defined as follows.



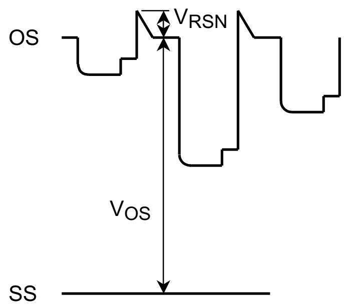
Note 6: V_{SAT} is defined as minimum saturation output of all effective pixels.

Note 7: Definition of SE: $SE = \frac{V_{SAT}}{R_{B/W}}$ (lx・s)

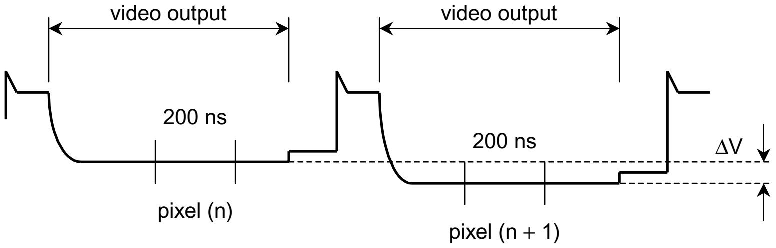
Note 8: V_{DRK} is defined as average dark signal voltage of all effective pixels. DSNU is defined as different voltage between V_{DRK} and V_{MDK} when V_{MDK} is maximum dark signal voltage.



Note 9: DC signal output voltage and reset noise is defined as follows, but reset noise is a fixed pattern noise.



Note 10: Random noise is defined as the standard deviation (sigma) of the output level difference between two adjacent effective pixels under no illumination (i.e. dark conditions) calculated by the following procedure.



Output waveform (effective pixels under dark condition)

(1) Two adjacent pixels (pixel n and n + 1) in one reading are fixed as measurement points.
(2) Each of the output level at video output periods averaged over 200 ns period to get V (n) and V (n + 1).
(3) V (n + 1) is subtracted from V (n) to get ΔV.

$$\Delta V = V(n) - V(n+1)$$

(4) The standard deviation of ΔV is calculated after procedure (2) and (3) are repeated 30 times (30 readings)

$$\overline{\Delta V} = \frac{1}{30}\sum_{i=1}^{30}|\Delta V i| \qquad \sigma = \sqrt{\frac{1}{30}\sum_{i=1}^{30}(|\Delta V_i| - \overline{\Delta V})^2}$$

(5) Procedure (2), (3) and (4) are repeated 10 times to get sigma value.
(6) 10 sigma values are averaged.

$$\overline{\sigma} = \frac{1}{10}\sum_{j=1}^{10}\sigma_j$$

(7) $\overline{\sigma}$ value calculated using the above procedure is observed $\sqrt{2}$ times larger than that measured relative to the ground level. So we specify random noise as follows.

$$N_{D\sigma} = \frac{1}{\sqrt{2}}\overline{\sigma}$$

Operating Condition

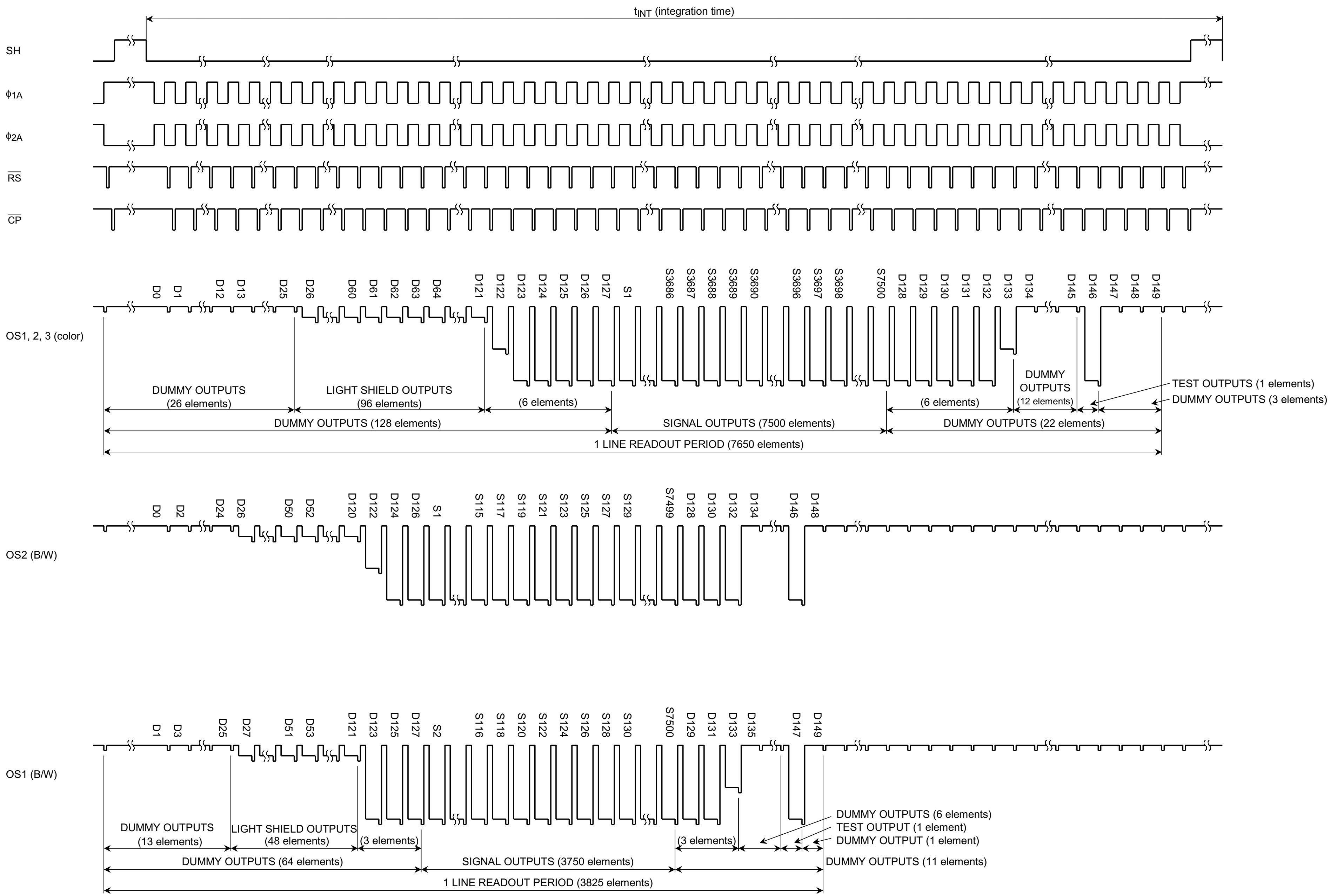
Characteristics		Symbol	Min	Typ.	Max	Unit	Note
Clock pulse voltage	"H" Level	$V_{\phi A}$	4.5	5.0	5.5	V	
	"L" Level		0	—	0.5		
Shift pulse voltage	"H" Level	V_{SH}	4.5	5.0	5.5	V	
	"L" Level		0	—	0.5		
Reset pulse voltage	"H" Level	$V_{\overline{RS}}$	4.5	5.0	5.5	V	
	"L" Level		0	—	0.5		
Clamp pulse voltage	"H" Level	$V_{\overline{CP}}$	4.5	5.0	5.5	V	
	"L" Level		0	—	0.5		
Switch pulse voltage	"H" Level	$V_{\overline{SW}}$	4.5	5.0	5.5	V	
	"L" Level		0	—	0.5		
Power supply voltage		V_{OD}	11.4	12.0	13.0	V	

Clock Characteristics (Ta = 25°C)

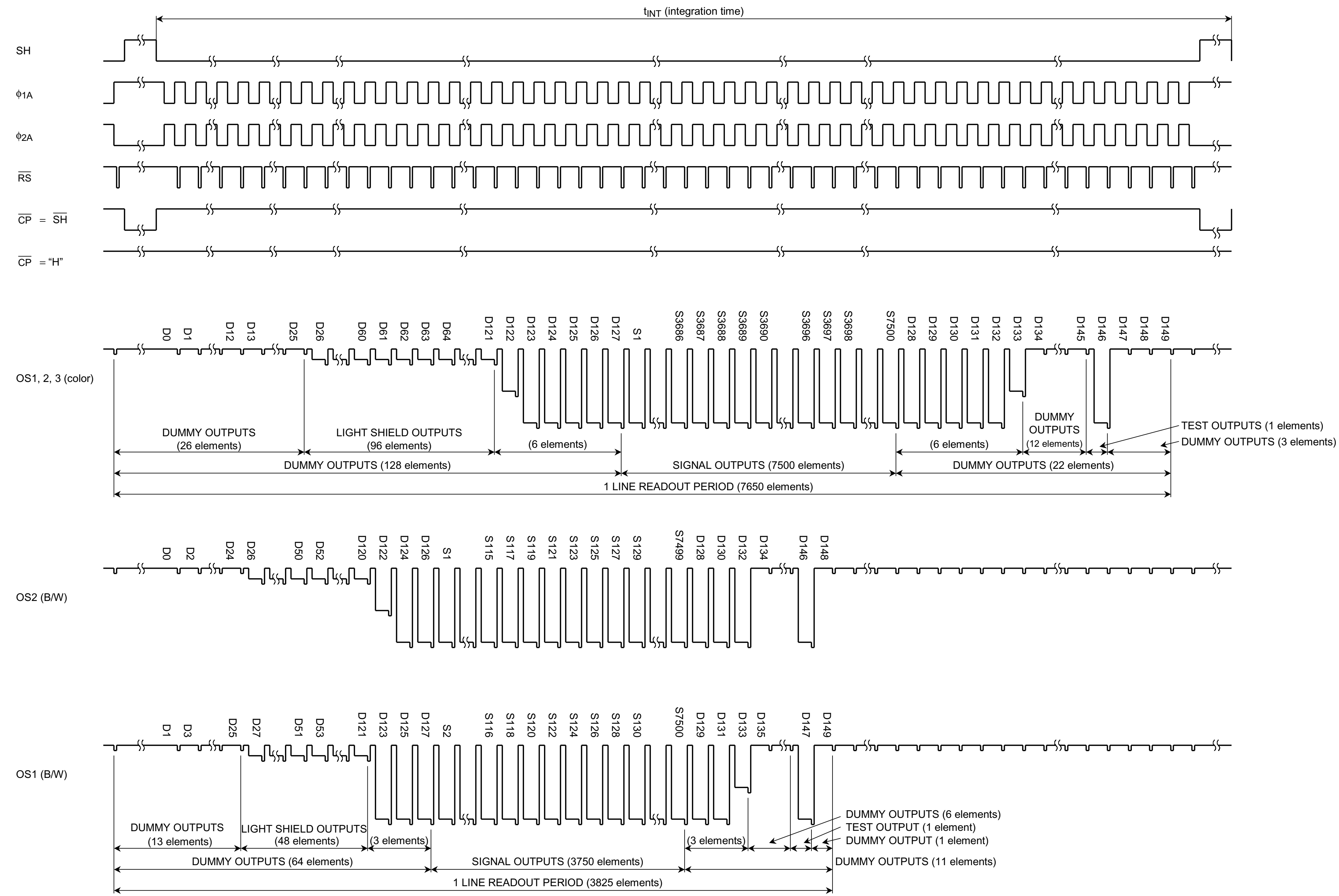
Characteristics	Symbol	Min	Typ.	Max	Unit
Clock pulse frequency	f_{ϕ}	0.3	1.0	12	MHz
Reset pulse frequency	$f_{\overline{RS}}$	0.3	1.0	12	MHz
Clamp pulse frequency	$f_{\overline{CP}}$	0.3	1.0	12	MHz
Clock1 capacitance (Note 11)	$C_{\phi 1}$	—	260	390	pF
Clock2 capacitance (Note 11)	$C_{\phi 2}$	—	210	315	pF
Shift gate capacitance	C_{SH}	—	30	60	pF
Reset gate capacitance	$C_{\overline{RS}}$	—	10	40	pF
Clamp gate capacitance	$C_{\overline{CP}}$	—	10	40	pF
Switch gate capacitance	$C_{\overline{SW}}$	—	10	40	pF

Note 11: V_{OD} = 12 V

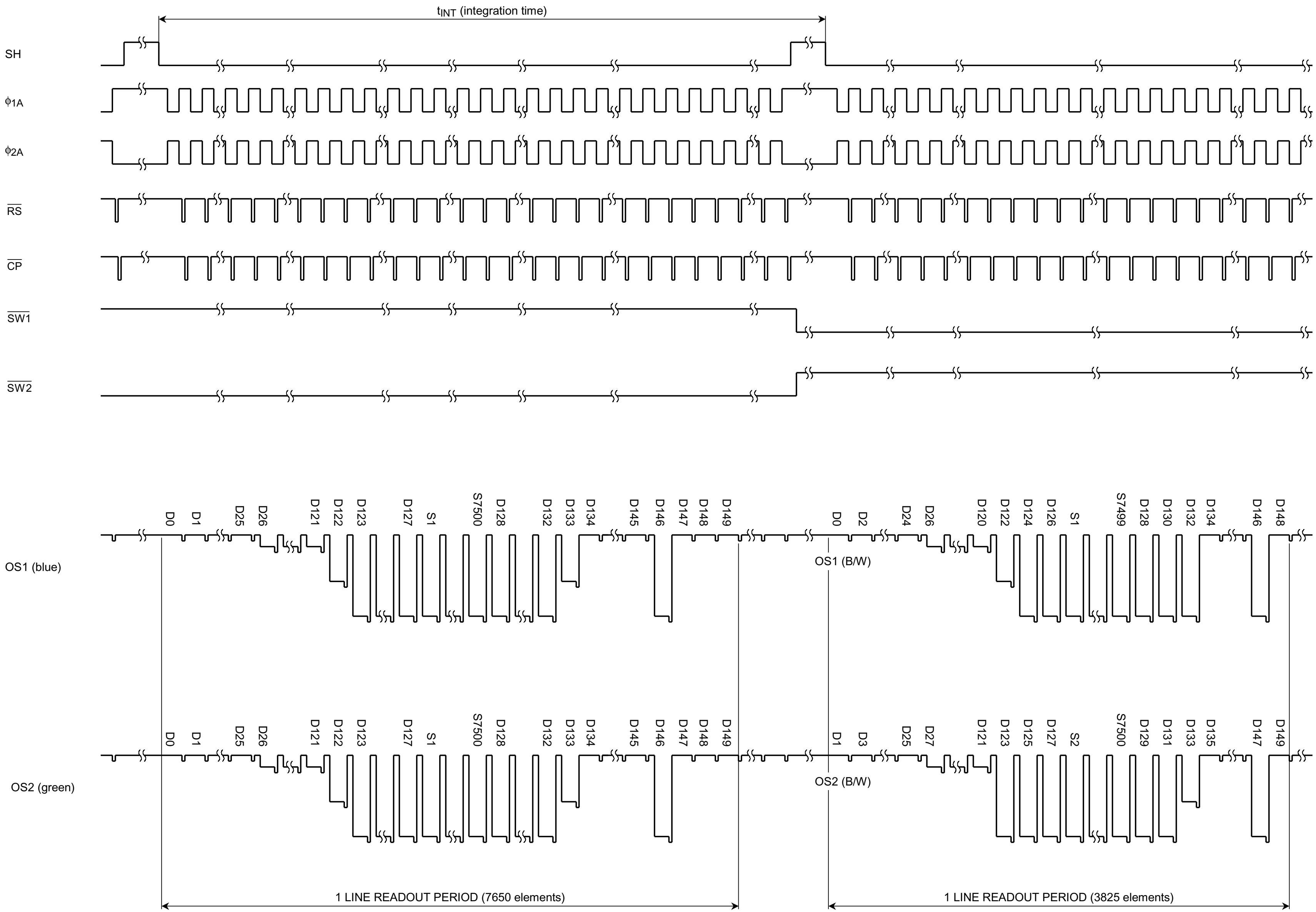
Timing Chart 1: Bit Clamp Mode (color or B/W mode)



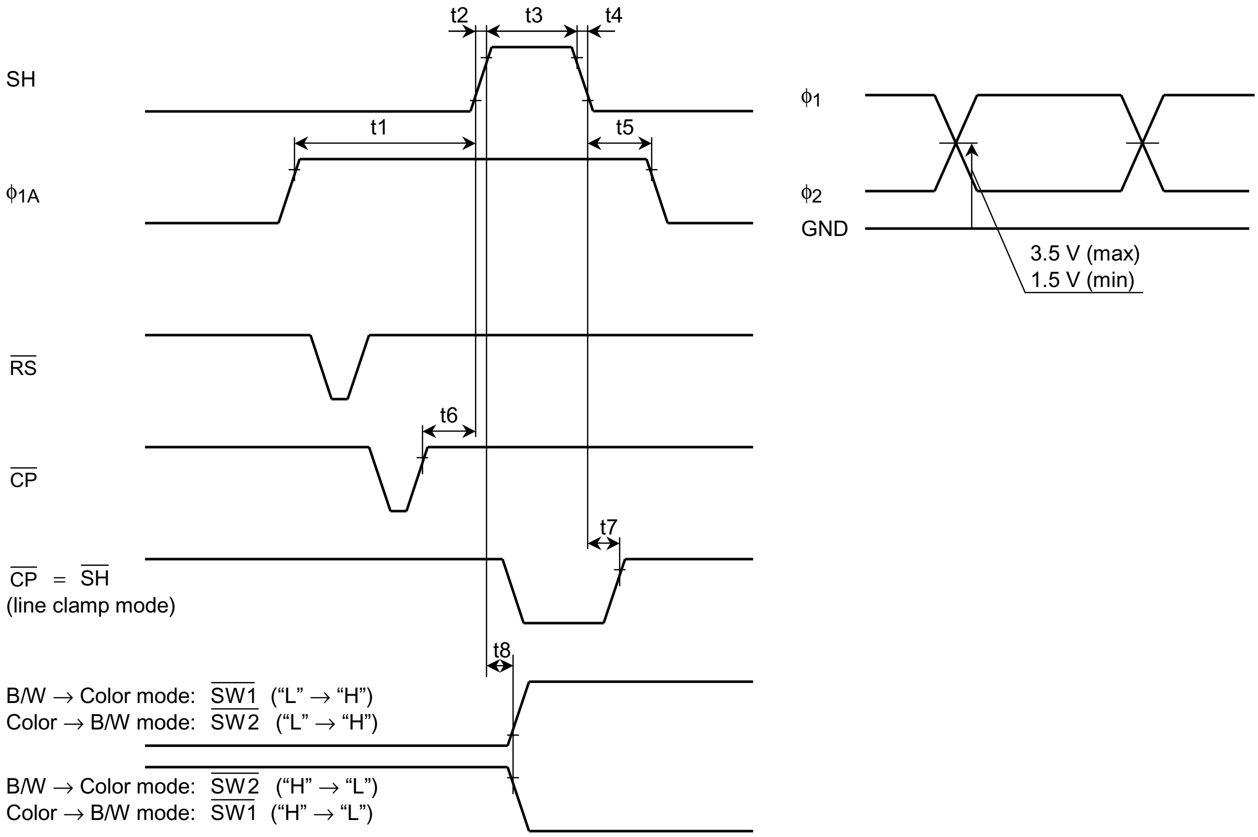
Timing Chart 2: Line Clamp Mode (color or B/W mode)

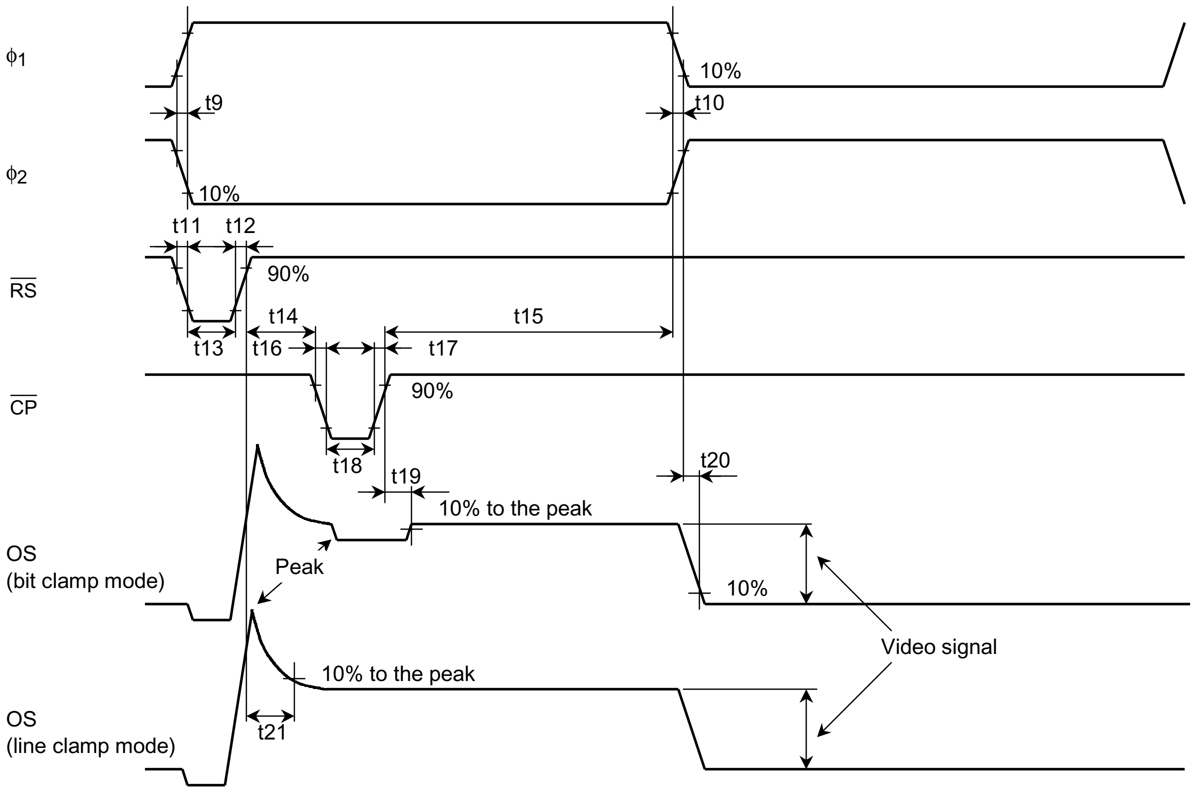


Timing Chart 3 (color → B/W mode)



Timing Requirements





Timing Requirements (cont.)

Characteristics	Symbol	Min	Typ. (Note 12)	Max	Unit
Pulse timing of SH and $\phi 1$	t1	120	1000	—	ns
	t5	800	1000	—	
SH pulse rise time, fall time	t2, t4	0	50	—	ns
SH pulse width	t3	3000	5000	—	ns
Pulse timing of SH and $\overline{CP}$	t6	200	500	—	ns
Pulse timing of SH and $\overline{CP}$ (line clamp mode)	t7	10	100	—	ns
Pulse timing of SH and $\overline{SW}$	t8	100	500	t3 – 100	ns
$\phi 1$, $\phi 2$ pulse rise time, fall time	t9, t10	0	50	—	ns
$\overline{RS}$ pulse rise time, fall time	t11, t12	0	20	—	ns
$\overline{RS}$ pulse width	t13	10 (20)	80	—	ns
Pulse timing of $\overline{RS}$ and $\overline{CP}$	t14	0	40	—	ns
Pulse timing of ϕ_{1A}, ϕ_{2A} and $\overline{CP}$	t15	0	20	—	ns
$\overline{CP}$ pulse rise time, fall time	t16, t17	0	20	—	ns
$\overline{CP}$ pulse width (Note 13)	t18	30 (3000)	80 (5000)	—	ns
Reference level settle time (bit clamp mode)	t19	—	20	40 (Note 16)	ns
Video data delay time (Note 14)	t20	—	20	40 (Note 15)	ns
Reference level settle time (line clamp mode)	t21	—	30	50 (Note 16)	ns

Note 12: Typ. is the case of $f_{\overline{RS}}$ = 1.0 MHz.

Note 13: Line clamp Mode inside ( ).

Note 14: Load Resistance is 100 kΩ.

Note 15: Typical settle time to about 1% of final value.

Note 16: Typical settle time to about 1% of the peak.

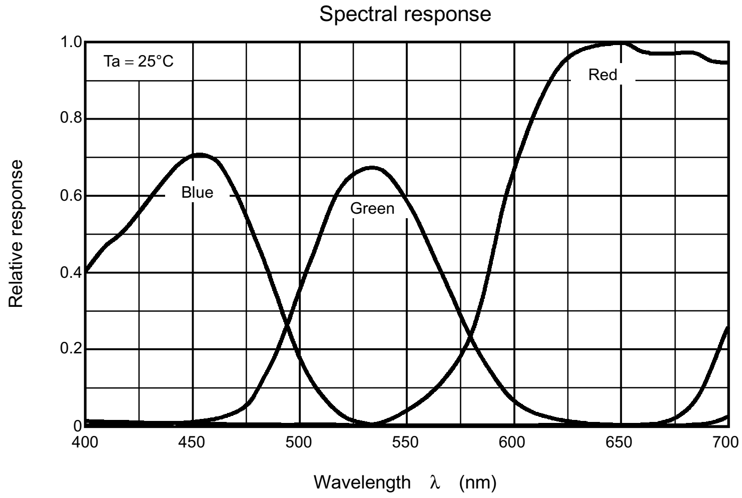
Clamp Mode

Clamp Means	$\overline{CP}$ Input Pulse
Bit clamp	$\overline{CP}$ Pulse
Line clamp	“H” or $\overline{SH}$

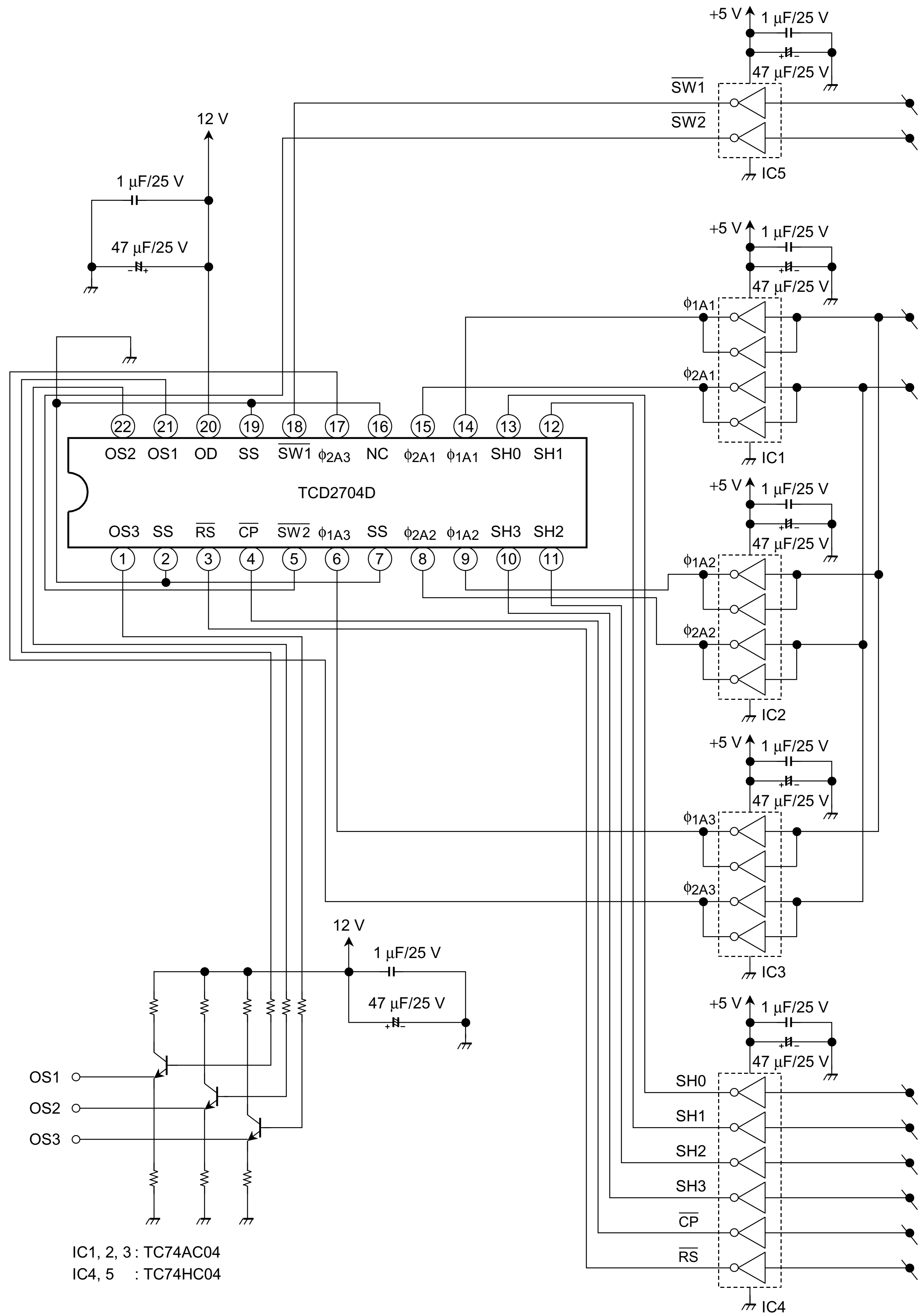
Changeover Switch Mode

Output Type	$\overline{SW1}$ Input Pulse	$\overline{SW2}$ Input Pulse
Color	“H”	“L”
B/W	“L”	“H”

Typical Spectral Response



Typical Drive Circuit



Caution

1. Window Glass

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.

Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N2. Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

2. Electrostatic Breakdown

Store in shorting clip or in conductive foam to avoid electrostatic breakdown.

CCD Image Sensor is protected against static electricity, but interior puncture mode device due to static electricity is sometimes detected. In handing the device, it is necessary to execute the following static electricity preventive measures, in order to prevent the trouble rate increase of the manufacturing system due to static electricity.

a. Prevent the generation of static electricity due to friction by making the work with bare hands or by putting on cotton gloves and non-charging working clothes.
b. Discharge the static electricity by providing earth plate or earth wire on the floor, door or stand of the work room.
c. Ground the tools such as soldering iron, radio cutting pliers of or pincer.

It is not necessarily required to execute all precaution items for static electricity.

It is all right to mitigate the precautions by confirming that the trouble rate within the prescribed range.

3. Incident Light

CCD sensor is sensitive to infrared light. Note that infrared light component degrades resolution and PRNU of CCD sensor.

4. Lead Frame Forming

Since this package is not strong against mechanical stress, you should not reform the lead frame.

We recommend to use a IC-inserter when you assemble to PCB.

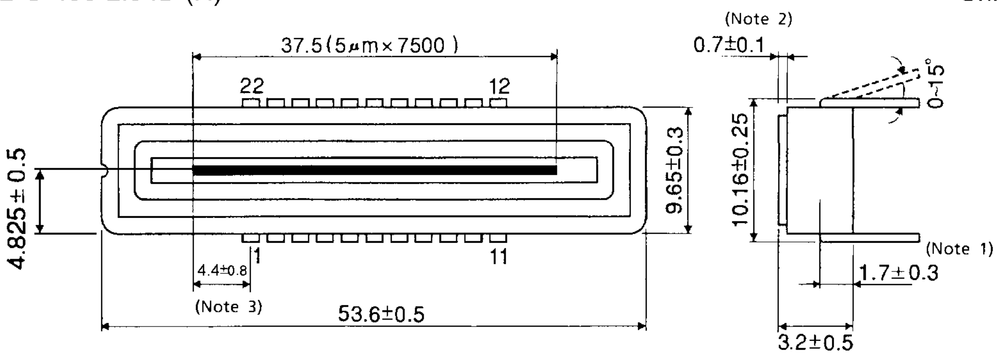
5. Soldering

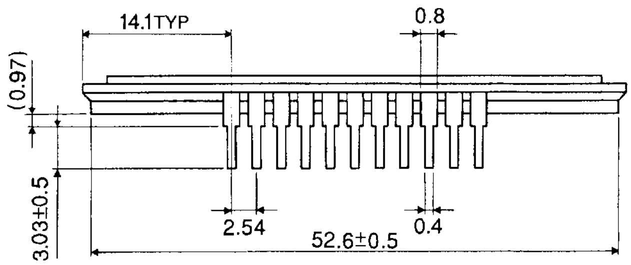
Soldering by the solder flow method cannot be guaranteed because this method may have deleterious effects on prevention of window glass soiling and heat resistance.

Using a soldering iron, complete soldering within ten seconds for lead temperatures of up to 260°C, or within three seconds for lead temperatures of up to 350°C.

Package Dimensions

WDIP22-G-400-2.54D (H) Unit: mm





(Note 1) : TOP OF CHIP TO BOTTOM OF PACKAGE.
(Note 2) : GLASS THICKNESS (n = 1.5)
(Note 3) : No.1 SENSOR ELEMENT (S1) TO EDGE OF No.1 PIN.

Weight: 5.2 g (typ.)

RESTRICTIONS ON PRODUCT USE

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